## REMARKS

The specification has been objected to because the Abstract does not comply with proper language requirements.

The specification has been objected to for having typographical errors.

Claims 5, 9, 15, and 19 have been objected to for having typographical errors.

Claims 1, 3, 4, 11, 13, and 14 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,515,548 to Matsumoto et al. ("Matsumoto").

Claims 2, 10, 12, and 20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Matsumoto in view of U.S. Patent Publication No. 2003/0208286 to Abercrombie ("Abercrombie").

Claims 6-8 and 16-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Matsumoto in view of U.S. Patent Publication No. 2005/0022081 to Syed ("Syed").

Claims 5, 9, 15, and 19 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in dependent form including all of the limitations of the base claim and any intervening claims.

Claims 1-20 remain pending.

### Objections to the Abstract

The Office Action states that the Abstract has been objected to because it does not comply with proper language requirements. The Abstract has been amended to replace the word "comprises" with the word "includes".

Applicant submits that this objection has now been overcome.

Objections to the Specification

The Office Action states that the specification has been objected to because of typographical errors. The specification has been amended to correct the typographical errors.

Applicant submits that this objection has now been overcome.

Objection to claims 5, 9, 15, and 19

The Office Action states that Claims 5, 9, 15, and 19 have been objected to for having typographical errors. Claims 5, 9, 15, and 19 have been amended to correct the typographical errors, as suggested by the Examiner. Further, claims 5 and 15 have been amended to correct typographical errors not pointed out by the Examiner. Specifically, the word "tempertue" was replaced by the work "temperature".

Applicant submits that this objection is now overcome.

Rejection of Claims 1, 3, 4, 11, 13, and 14 under 35 U.S.C. §102(b)

The Office Action states that Matsumoto teaches a method of testing and measuring an IC chip comprising, prior to manufacturing, determining a temperature sensitive parameter of the chip that is predictable with change of temperature. The method further comprises, during manufacturing, measuring the temperature sensitive parameter of the chip during testing of the chip, and measuring the chip temperature during or following the measurement of the temperature sensitive parameter. The method still further comprises, during manufacturing, determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Applicant respectfully disagrees with the characterization and interpretation of Matsumoto. Matsumoto teaches a temperature compensated oscillator, its manufacturing method, and integrated circuit for the temperature compensated oscillator. A crystal resonator is electrically connected to an oscillator circuit. The oscillator circuit also includes a switch, which selectively establishes communication between an A/D converter and non-volatile memory or between the A/D converter and a sequential comparing register. Before the oscillator circuit can be used, it must be calibrated. The oscillator circuit is calibrated by obtaining compensation data for the crystal resonator for a range of temperatures, and the compensation data is stored in the non-volatile memory. During calibration, an external reference frequency signal is electrically connected to the oscillator circuit. The switch is positioned to establish a connection between the A/D converter and the sequential comparing register. The compensation data is then obtained by comparing the external reference frequency to the frequency of the crystal resonator for a range of temperatures, and stored in the non-volatile memory. After the calibration is complete, the switch is positioned to establish a connection between the A/D converter the non-volatile memory, and the external reference frequency signal is disconnected from the oscillator circuit. Thereafter, during operation, compensation data for the particular operating temperature is retrieved from the non-volatile memory to correct the operation of the crystal resonator.

Unlike Applicant's invention, Matsumoto does not teach determining a temperature sensitive parameter of the chip that is <u>predictable</u> with change of temperature. The process of obtaining the compensation data is executed to determine how the oscillator will behave as a function of temperature. In other words, the oscillator frequency response is not <u>predictable</u> with change of temperature. Further, while the oscillator frequency can be determined if the

temperature is known (after the calibration process has been completed), the temperature can be determined if the oscillator frequency is know.

In contrast, Applicant's independent claim 1 teaches a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is predictable with change of temperature. Specifically, Applicant's invention involves using the relationship between the chip's maximum operating frequency and the chip's temperature. This relationship is predictable, which means if one of the parameters is known, the other can be determined. In other words, the temperature sensitive parameter that is predictable with change of temperature is the chip's maximum operating frequency, Fmax (see paragraph 0010).

Applicant's independent claim 1 further teaches determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature. Specifically, Applicant's invention involves determining an adjusted frequency based on measured frequency, measured chip temperature, and the determined (predictable) rate of change of the frequency with respect to the change in temperature (see paragraph 0018).

Unlike Applicant's invention, Matsumoto also does not teach or suggest, during manufacturing, determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature. Matsumoto instead teaches obtaining compensation data for the crystal resonator and then compensating the variation in the crystal resonator frequency with the compensating

data at a particular temperature, wherein the compensating data was obtained point by point for a range of temperatures (i.e. a parameter that is not predictable). Matsumoto then adjusts the temperature dependent parameter, namely the crystal oscillator frequency, by applying the compensation data obtained for the particular temperature. Further, the adjustment to the crystal resonator frequency is executed during a calibration phase, not during a manufacturing phase. At the time the compensation data is obtained, the oscillator circuit has already been manufactured.

In view of the foregoing, it is respectfully submitted that Matsumoto does not teach or suggest the subject matter recited in independent claim 1. Specifically, Matsumoto does not teach or suggest a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is predictable with change of temperature, and determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Independent claim 11 recites limitations similar to those recited in independent claim 1, and therefore is patentably distinct over Matsumoto for at least those reasons provided for independent claim 1.

Claims 3, 4, 13, and 14, which depend directly or indirectly from the independent claims 1 and 11, incorporate all of the limitations of the corresponding independent claim and are therefore patentably distinct over Matsumoto for at least those reasons provided for independent claims 1 and 11.

Rejection of Claims 2, 10, 12, and 20 under 35 U.S.C. §103(a)

The Office Action States that Matsumoto teaches the subject matter of claims 1 and 11, but does not mention expressly, with respect to claims 2 and 12, sorting the chip into a category based upon the adjusted temperature sensitive parameter of the chip. Further, with respect to claims 10 and 20, Matsumoto does not mention testing the chip in production tests to classify each chip into different categories of the temperature sensitive parameter. The Office Action further states that Abercrombie discloses a method of manufacturing integrated circuits, and teaches sorting an integrated circuit chip into a category based upon a temperature sensitive manufacturing parameter of the chip, and testing the chip in production tests to classify each chip into different categories of the temperature sensitive parameter.

As previously discussed, Matsumoto does not teach or suggest the subject matter recited in Applicant's independent claims 1 and 11. Specifically, Matsumoto does not teach or suggest a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is predictable with change of temperature, and determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Further, because Matsumoto does not teach or suggest the subject matter recited in independent claims 1 and 11, and because Abercrombie does not teach or suggest the elements of claims 1 and 11 that Matsumoto is missing, Abercrombie is irrelevant.

In view of the foregoing, it is respectfully submitted that Matsumoto and Abercrombie, whether taken alone or in combination, do not teach or suggest the subject matter recited in

claims 1 and 11 as each of these references fails at least to teach or suggest a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is <u>predictable</u> with change of temperature, and determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Claims 2, 10, 12, and 20, which depend directly or indirectly from the independent claims 1 and 11, incorporate all of the limitations of the corresponding independent claim and are therefore patentably distinct over Matsumoto in view of Abercrombie for at least those reasons provided for claims 1 and 11.

<u>Rejection of Claims 6-8 and 16-18 under 35 U.S.C. §103(a)</u>

The Office Action states that Matsumoto teaches the subject matter of claims 1 and 11, but does not but does not mention expressly, with respect to claims 6 and 16, determining a change of the temperature sensitive parameter of the chip that is the chip power consumption. Further, with respect to claims 7 and 17, Matsumoto does not mention determining a change of the temperature sensitive parameter of the chip that is the chip I/O timings. Further still, with respect to claim 8 and 18, Matsumoto does not mention determining maximum and minimum voltage test which measure the highest and lowest possible voltages at which a product will operate. The Office Action further states that Syed discloses test systems for testing integrated circuit devices and for calibrating associated system and methods, and teaches determining a change of the temperature sensitive parameter of the chip that is the chip power consumption, determining a change of the temperature sensitive parameter of the chip that is the chip I/O

timings, and determining maximum and minimum voltage test which measure the highest and lowest possible voltages at which a product will operate.

As previously discussed, Matsumoto does not teach or suggest the subject matter recited in Applicant's independent claims 1 and 11. Specifically, Matsumoto does not teach or suggest a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is predictable with change of temperature, and determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Further, because Matsumoto does not teach or suggest the subject matter recited in independent claims 1 and 11, and because Syed does not teach or suggest the elements of claims 1 and 11 that Matsumoto is missing, Syed is irrelevant.

In view of the foregoing, it is respectfully submitted that Matsumoto and Syed, whether taken alone or in combination, do not teach or suggest the subject matter recited in claims 1 and 11 as each of these references fails at least to teach or suggest a method of testing and measuring an IC chip including, prior to manufacturing, determining a change of a temperature sensitive parameter of the chip that is predictable with change of temperature, and determining an adjusted temperature sensitive parameter of the chip based upon the measured temperature sensitive parameter of the chip during testing, the measured chip temperature, and the determined change of the temperature sensitive parameter of the chip with temperature.

Claims 6-8 and 16-18, which depend directly or indirectly from the independent claims 1 and 11, incorporate all of the limitations of the corresponding independent claim and are

therefore patentably distinct over Matsumoto in view of Syed for at least those reasons provided for independent claims 1 and 11.

## Conclusion

In view of the foregoing, applicants respectfully requests reconsideration, withdrawal of all rejections, and allowance of all pending claims in due course.

Respectfully submitted,

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